

IN THE CLAIMS

Claims 1-20 (canceled)

Claim 21 (new): A method for making a semiconductor device comprising:

forming on a substrate a dielectric layer that has a dielectric constant that is greater than the dielectric constant of silicon dioxide;

forming a sacrificial layer on the dielectric layer;

removing the sacrificial layer; and then

forming a gate electrode on the dielectric layer.

Claim 22 (new): The method of claim 21 further comprising transporting impurities from the dielectric layer to the sacrificial layer prior to removing the sacrificial layer.

Claim 23 (new): The method of claim 22 wherein the dielectric layer is a high-k gate dielectric layer that has a dielectric constant that is greater than about 8.

Claim 24 (new): The method of claim 23 wherein the high-k gate dielectric layer is formed by atomic layer chemical vapor deposition, and wherein the high-k gate dielectric layer comprises a material selected from the group consisting of hafnium oxide, lanthanum oxide, zirconium oxide, zirconium silicon oxide, titanium oxide, tantalum oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate.

Claim 25 (new): The method of claim 24 wherein the sacrificial layer comprises a titanium nitride layer.

Claim 26 (new): The method of claim 25 wherein the titanium nitride layer is annealed to cause the impurities to be transported from the dielectric layer to the titanium nitride layer.

Claim 27 (new): The method of claim 26 wherein the gate electrode comprises polysilicon.

Claim 28 (new): A method for making a semiconductor device comprising:

forming a high-k gate dielectric layer on a substrate, the high-k gate dielectric layer including impurities;

removing the impurities from the high-k gate dielectric layer; and then

forming a gate electrode on the high-k gate dielectric layer.

Claim 29 (new): The method of claim 28 further comprising forming a sacrificial layer on the high-k gate dielectric layer, and transporting the impurities from the high-k gate dielectric layer to the sacrificial layer.

Claim 30 (new): The method of claim 29 wherein the substrate comprises silicon.

Claim 31 (new): The method of claim 30 wherein the high-k gate dielectric layer is formed by atomic layer chemical vapor deposition, and is between about 20 angstroms and about 60 angstroms thick.

Claim 32 (new): The method of claim 31 wherein the high-k gate dielectric layer comprises a material selected from the group consisting of hafnium oxide, zirconium oxide, titanium oxide, and aluminum oxide.

Claim 33 (new): The method of claim 32 wherein the sacrificial layer is between about 10 angstroms and about 50 angstroms thick.

Claim 34 (new): The method of claim 33 wherein the sacrificial layer is annealed by heating that layer at between about 500°C and about 1,000°C for between about 5 minutes and about 20 minutes.

Claim 35 (new): The method of claim 34 wherein the sacrificial layer is removed using a wet etch process that is selective for the sacrificial layer over the material used to make the high-k dielectric layer.

Claim 36 (new): The method of claim 35 wherein gate electrode comprises polysilicon.

Claim 37 (new): The method of claim 28 wherein the gate electrode is formed directly on the high-k gate dielectric layer.

Claim 38 (new): The method of claim 21 wherein the gate electrode is formed directly on the dielectric layer.